REMARKS

Claim 1 is amended and claims 4, 6 and 9 have been cancelled without prejudice or disclaimer. Claims 1-3, 5, 7, 8, 10 and 11 are pending in the application. Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claim 1 is amended herein to incorporate features of original claim 4. In addition, claim 1 has been amended to specify that the bipolar transistor claimed is suitable for operation as a saturated switch. Basis for this amendment may be found in original claim 4 and on page one of the application as filed in the second paragraph where it is made clear that an embodiment of a bipolar transistor is to be operated as a saturated switch, where a small base current is used to switch on a much larger collector to emit a current, the size of this current being determined by the voltage supply and the load resistance connected to either the collector or the emitter.

Claims 1 and 10 had been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Claims 2-5 and 7-16 had been rejected as being directly or indirectly dependent on independent claims 1 and 10. The Examiner stated that amended claim 1 and new claim 10 recite "when the metal layer has a thickness less than 3 microns." The Examiner further stated that it is unclear to the Examiner as to what metal is being used which would have the material dependent property of 500mOhms.mm^2 in specific area resistance. The Examiner stated that the claims are not examinable since the metal is not identified either in the claims or in the specification pertaining to the material property of specific area resistance. The rejection is respectfully traversed, in view of the following remarks.

It is submitted that the claims of the present application are enabled and comply with the requirements of 35 U.S.C. 112, first paragraph. It is believed that the rejection is based on the Examiner's apparent misunderstanding of the phrase "specific area resistance" as commonly used in connection with transistor technology.

For a bipolar transistor operating as a saturated switch, it is desirable to have a specific area resistance which is a low as possible. The specific area resistance is a measure used to assess such switch transistors and corresponds to the resistance of the device multiplied by its

area. This is a well known parameter used to assess transistors operating as saturated switching devices. It is typically desired that this is as low as possible.

A low area for the device can be desirable, but this will naturally lead to an increase in the resistance across the device as the area is reduced. A low resistance is good to prevent heating etc., but in order to obtain low resistance, prior devices have used high surface areas. Hence, a device which can give both a low resistance and a low surface area can be advantageous over what has already been provided in the prior art in the field of transistors used as saturated switches.

The parameter of (resistance)x(surface area) is well known for MOSFETs but is also applicable to bipolar transistors used as saturated switches. The resistance is not an incremental resistance but is defined at saturation of the device. Hence, the resistance corresponds to the voltage at saturation divided by the saturation current. Hence, a 1A current at a saturation voltage of 30mV would correspond to an effective resistance of 30mOhm.

Thus, in the context of bipolar transistors, a specific area resistance would be understood by one of ordinary skill in the art as the resistance of the device multiplied by its area. The rejection, on the other hand, appears to focus on the metal material of the metal layer. In particular, the Examiner stated that the claims are not examinable since *the metal is not identified either in the claims or in the specification pertaining to the material property of specific area resistance*.

However, the patent specification describes embodiments (e.g., with reference to Fig. 1) of bipolar transistor configurations that meet the claimed structure and parameters, including the specific area resistance and metal layer thickness. The present application describes embodiments that employ some conventional materials (see, e.g., page 5, lines 23-27). One of ordinary skill in the art would understand that the metal employed in the metal contacts 6 and 7 could be conventional metal contact materials. Accordingly, in the context of common knowledge in the industry of metals used for contact layers, and in the context of the conventional industry meaning of specific area resistance (resistance of the device multiplied by its area), it is submitted that the claims are enabled and in compliance with 35 U.S.C. 112, first

paragraph. In addition, claim 1, as amended, no longer includes the phrase "when the metal layer has a thickness less than 3μm."

The skilled person in the field of bipolar transistors would be aware that the typical metallization used is Aluminium, or an alloy of Aluminum containing 95% Aluminium or more. Alloy elements such as Silicon (up to 2%) to reduce spikes through shallow junctions, and Copper (up to 1%) to improve electro-migration may be also incorporated into the metallization.

The use of Aluminium alloys is well known and cited in the following public domain literature:

1) Phillips, Alvin B. "Transistor Engineering and Introduction to Integrated Circuits", McGraw-Hill, 1962, p23-24

2) Streetman, Ben G. "Solid State Electronic Devices, 2nd Edition", Prentice/Hall Inc., 1980 p131-132, p239-241

3) Leaver, Keith Drummond "Microelectronic Devices", Imperial College Press, 1997, p209

4) EP 0 341 221 A2, SGS-Thompson Microelectronics, pub. 8/11/89, p4, col 5, line 8.

The skilled person would have no difficulty, using aluminium based metallization, or any other suitable metal, in putting the claimed invention into effect. It is not necessary for the skilled person to look into the specific area resistance of prior art metals used as contacts. The subject matter of the invention relates to the provision of a reduced voltage drop across the metal layer, by thickening the conventional metal layer, to improve the specific area resistance performance of the transistor device when operating as a saturated switch. Accordingly, it is submitted that the skilled person would understand the claimed invention and the original specification provides an enabling disclosure of the claimed invention. The rejection under 35 U.S.C. 112, first paragraph is respectfully traversed.

Furthermore, the claims recite an invention that is neither described nor suggested by the references of record. The patent specification refers to configurations of bipolar transistors that operate as saturated switches, wherein the emitter region defines a first surface, and the base

region extends through that surface in locations defined by apertures through the emitter region. This so-called matrix system is used to give a reduction in resistance for a fixed area of device by maximising the total area of emitter.

On page 2 of the application as filed it is explained that it is highly important to maintain a high emitter base area ratio in order to provide low resistance. By using the matrix design set out in the application as filed and specified in claim 1, it had previously been possible to obtain saturated switch transistors having a specific area resistance less than about 500mOhms.mm^2. However, prior to the present invention, the present Applicants had not been aware of any improvement in this specific area resistance of the transistor by further design optimisation in the prior art. Attempts to improve specific area resistance included wire contact resistance and parasitic resistance from the silicon substrate.

As more wires are added to reduce resistance, the wires take up surface area, which would lead to an increase in resistance at saturation. Accordingly, there tended to be an optimal value for the number of wires contacting the metal layer. Similarly, the parasitic resistance from the silicon substrate had been lowered as much as was possible.

What had not been realised in the prior art of record was that the voltage drop across the metal contacts running to the emitter regions was sufficient, in saturated switch bipolar transistors, to provide a situation where the transistor was not adequately biased at locations remote from the wire contacts. This leads to an increase in the effective resistance across the transistor at saturation which is much greater than might have been expected.

This problem arising from the voltage drop across metal contact strips had not been recognised in the prior art of record. However, the present inventors realised that this mechanism was leading to a significant contribution to the resistance of the bipolar transistor when at its saturated state. Effectively, the voltage drop across the metal contact meant that not all of the surface area of the transistor is switched into the "on" state and so not all of the transistor was operating in a fully saturated state. The present inventors not only recognized that problem, but also designed a solution to it: that of reducing the resistance of the metal contact by increasing

the metal thickness so that the voltage drop across the metal layer is reduced enabling the regions of base and emitter remote from the wire contact to be maintained in a saturated state.

A surprising effect of reducing the voltage drop across the metal layer is that this enables the surface area of a transistor to be reduced by 30%, for the same current, when in the saturated state, compared to prior designs with a conventional metal layer thickness of around 3 μm.

For example, consider the expected voltage drop across metal layers in a matrix transistor having thicknesses of 2 μm, 4 μm or 6 μm. An expected drop in voltage across a metal contact strip may be, for example, 1.06 millivolts for a 2 micron layer at 1 amp, 0.57 millivolts for a 4 micron layer at 1 amp and 0.39 millivolts for a 6 micron layer at 1 amp. These figures are in proportion to the reduced resistance arising from the increased thickness of the metal contact. In other words, the difference in voltage drop between the 2 micron layer and the 4 micron layer may be 0.49 millivolts, and between the 6 micron layer and the 2 micron layer, the difference may be 0.67 millivolts.

What had not been realised in the prior art of record was that the effect of this small difference in voltage drop has a considerably greater effect on the saturation voltage across the transistor. A saturation voltage with a 2 micron metal layer may be 31.59 millivolts compared to 25.9 millivolts for a 4 micron layer and 23.53 millivolts for a 6 micron layer. Comparing the 6 micron layer with the 2 micron layer gives a change in voltage of 8.1 millivolts in 31.59 millivolts at saturation, this corresponds to a 25% improvement in the specific area resistance of the device, considerably more than would have been expected from the minor reduction in the voltage drop across the metal layer arising from the increase in metal layer thickness.

In contrast, the Odekirk reference is concerned with ohmic and rectifying contacts for SiC devices, and makes mention of the specific contact resistances for Ni and TiC contacts as being $1x10^{-5}$ Ohm.cm^2 and $1x10^{-6}$ Ohm.cm^2. The specific area resistance of a metallic contact is not the same as the specific area resistance figure for a transistor acting as a saturated switch. There is no inherent disclosure in Oderkirkof a specific area performance such as that which is achievable with the bipolar transistor of the invention.

Other references cited by the Examiner are concerned with a direct reduction in the parasitic resistance arising from metal contacts and make no teaching whatsoever concerning the surprising reduction in voltage drop across a saturated switch transistor which can be achieved by a minor reduction in the resistance of the metallisation layer as conceived by the present inventors.

The Palara reference teaches a "finger structure" transistor which will have less than 50% of base covered by emitter. Such a design is not compatible with a low specific area resistance device. The device of Palara could never achieve the required performance, irrespective of the thickness of metal used. In fact, Palara teaches, in the abstract and elsewhere, to provide a high ballast resistance in series with the device, the exact opposite to the present application. Palara is concerned with power transistors, and not with transistors suitable for operation as a saturated switch. Thus, when looking to design a transistor suitable for operation as a saturated switch and having a low specific area resistance ***for the device***, the skilled person would not start from Palara.

Furthermore, the skilled person would not consider combining Palara with the teachings of Odekirk because Odekirk relates to a completely different technical field.

Odekirk makes no mention of bipolar transistors for use as a saturated switch, nor is there any teaching in Oderkirk concerning factors which affect the specific area performance of such devices. Instead, Odekirk is concerned with the completely different technical problem of provision of thermally stable contacts for SiC devices. As such, Oderkirk's specific resistance mentioned is specific ***contact*** resistance and not specific area resistance of the ***device***. As set out above, this specific figure of merit for device effective resistance times device area does not simply arise from arithmetic combination of specific contact resistance and specific device resistance. Instead, the voltage drop along the length of a finger-like metal contact can lead to the bipolar transistor not operating in saturated mode which leads to a considerably higher device resistance than would arise from a simple arithmetic approach. Odekirk makes no mention of this and is merely interested in the voltage drop across a metal contact, not along its length when used as a finger-like contact in a saturated switch device. .

Accordingly, it is submitted that the claims, as amended herein, comply with 35 U.S.C. 112, first paragraph, and remain distinguished from the prior art of record.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment instructions in EFS-Web being incorrect or absent, resulting in a rejected or incorrect credit card transaction, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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